## REMARKS

Reconsideration of the application is respectfully requested.

The following discussion addresses the issues in the order in which they have been raised in the Office Action.

**Claims Rejected Under 35 U.S.C. §112**

Claims 1-24 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

In particular, the Office Action expressed a concern with limitations such as "that memory", and "associated with that command" in claims 1, 12, 16 and 21. The Examiner's suggestion has been taken in this amendment, changing "that" to -- the -- in all effected claims. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §112 is respectfully requested.

**Claims Rejected Under 35 U.S.C. §102**

Claims 1-11 and 25-30 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0006729 issued to Pendurkar ("Pendurkar"). Applicants respectfully disagree with the rejection for the following reasons.

Beginning with claim 1, this independent claim now recites an apparatus having a processor to initiate a built-in self test for memories, with a serial bus that is coupled between the processor and each memory. The processor *loads a plurality of commands via the serial bus into a first one of the intelligence wrappers that bound the memories, where each of the commands comprises representations of a single march element and other data. The first intelligence wrapper contains control logic to decode the command from the processor and execute a set of test vectors of a march algorithm having a plurality of march elements.* Pendurkar does not teach or suggest such an apparatus.

According to the Office Action at page 4, Pendurkar discloses, in Fig. 5, memory arrays 508 in their respective cores, each associated with a respective memory BIST controller 510. A master BIST controller 504 asserts BIST enable signals for the arrays 508 to initiate testing operations. Although the Final Office Action refers to the bus 516 as being a *serial* bus that couples the master BIST controller 504 to the memory BIST controllers 510, Applicants respectfully disagree with this interpretation. That is because in both Fig. 3, which discloses a number of cores 308, as well as Fig. 5 which discloses an example core 500, Pendurkar only refers to "buses 318 and 320" for coupling the master BIST controller 304 to tap controller 302, and to an I/O terminal of each core 308. With respect to the core 500 in Fig. 5, Pendurkar merely refers to gating logic 501 as being "coupled to bus 318 via core I/O inputs, to bus 320 via CS inputs, and to tap controller 502 via bus 512." Similarly, "tap controller 502 is coupled to core mass memory BIST controller 504 via bus 514." **There is no textual description of whether the bus is a serial bus of a parallel bus**. If anything, one of ordinary skill would probably construe the depiction of the buses in Figs. 3 and 5 as **parallel or multi-drop** buses, rather than serial buses, **given the manner in which the intersecting line segments connect to different input and output ports of the components are joined at solid dots**. Accordingly, since Pendurkar merely refers to a "bus" which, at best, would be construed by one of ordinary skill as being a parallel or multi-drop bus, rather than a serial bus, reconsideration and withdrawal of the anticipation rejection is respectfully requested.

Claim 1 has been amended here to recite a further embodiment of the invention that is neither anticipated or obvious in view of Pendurkar. There is no teaching or suggestion in the cited art to modify Pendurkar such that *the first intelligence wrapper contains control logic to decode the command received over the serial bus from the processor and to execute a set of test vectors of* ***a march algorithm having a plurality of march elements, where each of the commands comprises representations of a single march element.*** Pendurkar does not suggest this specific level of control between the master BIST controller or the TAP controller, and a memory BIST controller. Support for such an amendment to claim 1 can be found in Applicants' Specification as filed, in paragraphs [0013] – [0014]. Although in Pendurkar, a control mode register 303b in the TAP controller (Fig. 3) stores a number of bits that indicate which algorithm (*e.g.*, which

particular march algorithm) to perform in the BIST, Pendurkar does not teach or suggest that each command comprise the representation of a **single march element** and where the march algorithm that is executed has **a plurality of march elements**.

Turning to the next independent claim, namely claim 12, this claim has been amended to overcome the rejection in view of Pendurkar, by reciting an apparatus in which memories are coupled to a BIST processor by a serial bus, where the processor is to initiate BIST for the memories via the serial bus, and the processor loads a number of commands via the serial bus into the first intelligence wrapper. Each command comprises representations of a single march element and other data. The first intelligence wrapper contains control logic to decode the command from the processor and to execute a set of test vectors of a march algorithm having a plurality of march elements. Pendurkar does not teach or suggest such an apparatus.

Pendurkar is silent on the type of bus that connects the master BIST controller to the cores and, hence, cannot teach or suggest the claimed *serial bus that is used to both initiate the BIST and to transfer commands from the processor to the intelligence wrappers*. Moreover, Pendurkar only refers to a register that contains a reference to a type of march algorithm but does not teach or suggest that each of the commands that are delivered to each intelligence wrapper comprise a single march element, where the subsequent BIST executes a march algorithm having a number of march elements.

As to claim 21, this claim has also been amended in a manner similar to claim 12 and is submitted as not being anticipated or obvious for at least the same reasons.

Turning now to claim 25, this claim as amended now recites *compressing information, to be used in a self-test of a memory embedded on a chip, into a command, wherein there is a march algorithm representation in said command*. The command is communicated via *a serial bus* to logic bounding the memory. The communicated command is received and *the compressed information is expanded by the logic bounding the memory, to perform a march algorithm as part of the self-test on the memory*. Although the Final Office Action at page 6 contends that Pendurkar's master BIST controller 504 "sends compressed information in the form of serial data", Applicants respectfully disagree with this interpretation. As explained above, Pendurkar does not fairly suggest the

*communication of commands via a serial bus to logic bounding the memory*. At best, Pendurkar would suggest to one of ordinary skill that a signal be sent over a parallel bus to each memory BIST controller, where this signal could indicate the type of march algorithm to be performed by the memory BIST controller. However, Pendurkar does not fairly teach or suggest to one of ordinary skill that *information to be used in a self-test of the memory be compressed into a command, wherein there is a march algorithm representation in said command*. Although in Pendurkar there is a register that can be programmed with an indication of which march algorithm to perform, this is not the same as *compressing information ... into a command, wherein there is a march algorithm representation in said command*.

The Final Office Action also points to paragraph 45 of Pendurkar, where this paragraph refers to the core 308 "decoding the instruction received from memory BIST controller 304". This, however, does not teach or suggest *expanding the compressed information in the received command by the logic bounding memory, to perform a march algorithm as part of the self-test on the memory*. Accordingly, for the above reasons, Applicants' claim 25 as amended here, is neither anticipated nor obvious in view of Pendurkar.

Claim 28 has been amended in a manner similar to claim 25, except that claim 28 refers to an apparatus in terms of means plus function elements, rather than a method. The functionality recited in claim 28 is respectfully submitted as not being taught or suggested in Pendurkar.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language.

## CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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By _____
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I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on April 16, 2007.

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*Margaux Rodriguez* *April 16, 2007*